SYSTEM AND METHOD FOR MEMORY INTERLEAVING USING CELL MAP WITH ENTRY GROUPING FOR HIGHER-WAY INTERLEAVING

Abstract of the Disclosure

A method of accessing a plurality of memories in an interleaved manner using a contiguous logical address space includes providing at least one map table. The at least one map table includes a plurality of entries. Each entry includes a plurality of entry items. Each entry item identifies one of the memories. A first logical address is received. The first logical address includes a plurality of address bits. The plurality of address bits includes a first set of address bits corresponding to a first set of entries in the at least one map table. A first entry in the first set of entries is identified based on the first set and a second set of the address bits. A first entry item in the first entry is identified based on a third set of the address bits. The memory identified by the first entry item is accessed.